WHAT IS CLAIMED IS:

1. A computer-implementable method of performing modulo division, using a dividend N and an n-bit divisor D to produce a remainder R, said method comprising:

when $D=2^n-1$ and $0 \leq N \leq (D-1)^2$, non-iteratively processing N mod D to produce the remainder R.

2. A computer-implementable method of performing modulo division, using a dividend N and an n-bit divisor D to produce a remainder R, said method comprising:

when $D=2^n-1$ and $0 \leq N \leq (D-1)^2$, performing N mod D to produce the remainder R, where a number of processing operations necessary to produce the remainder R is independent of n.

3. A computer-implementable method of performing modulo division, using a dividend N and an n-bit divisor D to produce a remainder R, said method comprising:

when $D=2^n-1$ and $0 \leq N \leq (D-1)^2$, summing the upper $\lceil \frac{n}{2} \rceil$ and lower $\lceil \frac{n}{2} \rceil$ bits of the dividend N to produce the remainder R.

4. The computer-implementable method of claim 1, further comprising the step of subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

5. The computer-implementable method of claim 2, further comprising the step of subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

6. The computer-implementable method of claim 3, further comprising the step of subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

7. The computer-implementable method of claim 1, wherein $n \geq 2$.

8. The computer-implementable method of claim 2, wherein $n \geq 2$.

9. The computer-implementable method of claim 8, wherein n≥2.

10. The computer-implementable method of claim 7, wherein n≥3.

11. The computer-implementable method of claim 8, wherein n≥3.

12. The computer-implementable method of claim 9, wherein n≥3.

13. An apparatus for performing modulo division, using a dividend N and an n-bit divisor D to produce a remainder R, said apparatus non-iteratively processing N mod D to produce the remainder R, when $D=2^n-1$ and $0\leq N\leq(D-1)^2$.

14. An apparatus for performing modulo division, using a dividend N and an n-bit divisor D to produce a remainder R, said apparatus performing N mod D to produce the remainder R, where a number of processing operations necessary to produce the remainder R is independent of n, when $D=2^n-1$ and $0\leq N\leq(D-1)^2$.

15. An apparatus for performing modulo division, using a dividend N and an n-bit divisor D to produce a remainder R, said apparatus summing the upper $\lceil \frac{n}{2} \rceil$ and lower $\lceil \frac{n}{2} \rceil$ bits of the dividend N to produce the remainder R, when $D=2^n-1$ and $0\leq N\leq(D-1)^2$.

16. The apparatus of claim 13, said apparatus subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

17. The apparatus of claim 14, said apparatus subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

18. The apparatus of claim 15, said apparatus subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

19. The apparatus of claim 13, wherein n≥2.

20. The apparatus of claim 14, wherein n≥2.

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~~21~~. The apparatus of claim ~~15~~, wherein n≥2.

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~~22~~. The apparatus of claim 19, wherein n≥3.

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~~23~~. The apparatus of claim ~~20~~, wherein n≥3.

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~~24~~. The apparatus of claim ~~21~~, wherein n≥3.

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~~25~~. The apparatus of claim ~~14~~, wherein said apparatus is a component of a Reed-Solomon coder.

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~~26~~. The apparatus of claim ~~15~~, wherein said apparatus is a component of a Reed-Solomon coder.

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27. The apparatus of claim ~~16~~, wherein said apparatus is a component of a Reed-Solomon coder.

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~~28~~. A computer program embodied in a computer readable medium for performing modulo division, using a dividend N and an n-bit divisor D to produce a remainder R, comprising:

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a summing code segment for summing the upper $\lceil \frac{n}{2} \rfloor$ and lower $\lceil \frac{n}{2} \rfloor$ bits of the dividend N to produce the remainder R, when $D=2^n-1$ and $0 \leq N \leq (D-1)^2$.

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~~29~~. The computer program of claim ~~28~~, further comprising a subtracting code segment for subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

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~~30~~. The computer program of claim ~~28~~, wherein n≥2.

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~~31~~. The computer program of claim ~~30~~, wherein n≥3.

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~~32~~. A computer signal for performing modulo division, using a dividend N and an n-bit divisor D to produce a remainder R, said computer signal comprising:

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a summing code segment for summing the upper $\lceil \frac{n}{2} \rceil$ and lower $\lceil \frac{n}{2} \rceil$ bits of the dividend N to produce the remainder R, when $D=2^n-1$ and $0 \leq N \leq (D-1)^2$.

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~~33~~. The computer signal of claim ~~32~~, further comprising a subtracting code segment for subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

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~~34~~. The computer signal of claim ~~32~~, wherein $n \geq 2$.

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45 ~~35~~. The computer signal of claim ~~34~~, wherein $n \geq 3$.

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